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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/979,572	BHARDWAJ ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001 and 15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *44-74* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-24 and 26-43* is/are rejected.

7)☐ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-43 have been considered. Claims 44-74 have been withdrawn as per Applicant's request. The Examiner assumes the election was made without traverse, since no arguments against the restriction requirement were not presented.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Revocation and new Power of Attorney as received on 09 February 2004 and Amendment as received on 15 April 2005.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 32-43 recite the limitation "the method recited" in line 1. There is insufficient antecedent basis for this limitation in the claim. There has been no previous occurrence of a method. Claim 1 is an apparatus claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-24, 27-32, and 34-43 are rejected under 35 U.S.C. 102(b) as being taught by Farber et al., U.S. Patent Number 4,516,203 (herein referred to as Farber).

9. Referring to claim 1, Farber has taught a processor comprising:

a. A data table for storing immediate data of immediate instructions (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2);

b. A program counter for storing an instruction address of an instruction, wherein the processor fetches the instruction from the instruction address in the program counter during program execution (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

c. An instruction decoder for decoding the instruction fetched by the processor (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

d. Wherein an immediate data from the data table is provided to the processor if the instruction is an immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines

16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

10. Referring to claims 2 and 10, Farber has taught

a. An instruction register coupled to the instruction decoder (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8);

b. The instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8). In regards to Farber, the I-stream Reader inherently has an instruction register in order to generate the outputs necessary.

11. Referring to claim 3, Farber has taught wherein the instruction register is coupled to the data table (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the instruction register provides an address of the immediate data in the data table when the immediate instruction is decoded by the instruction decoder (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

12. Referring to claims 4, 8, and 13, Farber has taught a data table addressing unit coupled to the instruction decoder and data table (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the data addressing unit providing an address of the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42;

column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

13. Referring to claims 5 and 9, Farber has taught wherein the data table addressing unit comprises a data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

14. Referring to claims 6 and 11, Farber has taught

a. Wherein the instruction register is coupled to the data table addressing unit (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

b. The instruction register passes addressing information to the instruction addressing unit to provide the address when the immediate instruction is decoded by the instruction decoder (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

15. Referring to claims 7 and 12, Farber has taught wherein the data table addressing unit comprises a data table pointer for storing the addressing information which serves as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

16. Referring to claim 14, Farber has taught wherein the data table addressing unit comprises an incrementor, the incrementor increments the address after the immediate data is provided to produce a new address for a new immediate instruction (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an incrementor to produce a new address.

17. Referring to claim 15, Farber has taught wherein the data table addressing unit comprises:

a. A data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. An incrementor, the incrementor increments the address in the data table pointer after the immediate data is provided to produce a new address in the data table pointer for a next immediate instruction executed by the processor (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an incrementor to produce a new address.

18. Referring to claim 16, Farber has taught wherein the incrementor comprises an adder, the adder is coupled to the data table pointer, the adder adds the address in the table pointer and an index to produce the new address (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an adder to produce a new address.

19. Referring to claim 17, Farber has taught wherein the index comprises a 1 (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column

9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

20. Referring to claim 18, Farber has taught wherein an addressing information is passed to the addressing unit, the addressing information comprises an index for indexing the address to produce a new address of another immediate data in the data table for another immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

21. Referring to claim 19, Farber has taught wherein addressing information is passed to the addressing unit, the addressing information comprises an index for indexing the address to produce a new address pointing to a next immediate data in the data table for a next immediate instruction fetched by the processor (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

22. Referring to claim 20, Farber has taught

a. An instruction register coupled to the instruction decoder and the data table addressing unit (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

b. The instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to

column 29, line 33; and Figure 8),

c. When the decoder decodes the immediate instruction, the instruction register passes the addressing information contained in the instruction to the data addressing unit (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

23. Referring to claim 21, Farber has taught wherein the data table addressing unit comprises:

a. A data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. An adder for adding the addressing information to the address after the immediate data is provided to produce a new address in the data table pointer for a next immediate instruction executed by the processor (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

24. Referring to claim 22, Farber has taught

a. An instruction register coupled to the instruction decoder (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

the instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

b. A data table addressing unit coupled to the data table and instruction register (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the instruction register passing relative addressing information contained in the instruction to the data table addressing unit when the decoder decodes the immediate instruction, the relative addressing information, which comprises an index and a format indicator, is used to provide an address of the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

25. Referring to claim 23, Farber has taught wherein the data addressing unit comprises a data table pointer containing a value,

a. If the format indicator comprises a post-format, the value serves as the address and after the immediate data is provided to the processor, the index is added to the value to produce a new value in the data table pointer for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15,

line 9; column 15, lines 28-64 and Figure 2), and

b. If the format indicator comprises a pre-format, the index is added to the value to produce the address to the immediate data and the address *is* incremented by 1 after the immediate data is provided to the processor to produce a new value in the data table pointer for the next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

26. Referring to claim 24, Farber has taught wherein the format indicator comprises a binary bit having a logic 1 and logic 0 value, the logic 1 indicating a pre-format and the logic 0 indicating the post-format (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

27. Referring to claim 31, Farber has taught a method of executing instructions in a processor, the method comprises separating immediate data of immediate instructions from an instruction stream (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

28. Referring to claim 32, Farber has taught wherein separating the immediate data from the

instruction stream comprises:

a. Fetching an instruction from a program (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8);

b. Decoding the instruction to determine a type of instruction (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

c. If the instruction comprises an immediate instruction, fetching an immediate data corresponding to the immediate instruction from a data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

29. Referring to claim 34, Farber has taught providing addressing information for fetching the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

30. Referring to claim 35, Farber has taught wherein the immediate instruction provides the addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

31. Referring to claim 36, Farber has taught storing the addressing information in a data table pointer (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

32. Referring to claim 37, Farber has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

33. Referring to claim 38, Farber has taught processing the relative addressing information by a data table addressing unit to generate an address for fetching the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

34. Referring to claim 39, Farber has taught wherein processing the relative addressing information comprises:

a. Using a value stored in a data pointer of the data addressing unit to serve as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. After fetching the immediate data, adding the relative addressing information to

the value to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

35. Referring to claim 40, Farber has taught wherein the addressing information comprises an index and a format indicator (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

36. Referring to claim 41, Farber has taught wherein processing the relative addressing information comprises:

a. If the format indicate comprises a post-format,

i. Using a value stored in a data pointer of the data addressing unit to serve as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2), and

ii. After fetching the immediate data, adding the index to the address to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9,

lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. If the format indicator comprises a pre-format,

i. Adding the index to the value to serve as the address for fetching the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2), and

ii. Incrementing the address after the immediate data is fetched to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 28, lines 37-38).

37. Referring to claim 42, Farber has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

38. Referring to claim 43, Farber has taught wherein providing the relative addressing information comprises:

a. Using a value in a data pointer to provide the addressing information to fetch the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58;

column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. Incrementing the value to provide a new addressing information for fetching another immediate data for a subsequent immediate instruction fetched by the processor (Farber column 28, lines 37-38).

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 26-30 and 33-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farber et al., U.S. Patent Number 4,516,203 (herein referred to as Farber), as applied to claims 1 and 32 respectively, in view of Vanek and Culp's "Static Analysis of Program Source Code using EDSA" ©1989 (herein referred to as Vanek).

41. Referring to claims 26 and 33, Farber has taught wherein the data table comprises immediate data stored to identify immediate instructions within a program (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2). Farber has not taught static flow analysis. Vanek has taught static flow analysis (Vanek page 192). A person of ordinary skill in the art at the time the invention was made to incorporate the static flow analysis to detect defects

(Vanek page 192). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the static flow analysis of Vanek in the device of Farber to detect errors.

42. Referring to claim 27, Farber has taught wherein an immediate instruction comprises addressing information to enable the processor to retrieve a corresponding immediate data to the immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

43. Referring to claim 28, Farber has taught wherein the addressing information comprises absolute addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

44. Referring to claim 29, Farber has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

45. Referring to claim 30, Farber has taught data addressing unit coupled to the data table, the data addressing unit receives the relative addressing information and produces an address to the corresponding immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58;

column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2)..

46. Referring to claims 34-43, since claim 34 is a multiple dependent claim, they would be rejected under 35 U.S.C. §103(a) when they are dependent off of claim 33. However, the art citations for the claim limitations are the same as when they are dependent off of claim 32. Please see the above rejections for claims 34-43 for more details on the prior art citations.

Allowable Subject Matter

47. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is an examiner's statement of reasons for indicating allowable subject matter: Claim 25 recites two adders with the specific inputs for each address and a multiplexor with its three specific inputs, which has not been found in association with this type of immediate data addressing and tabling scheme.

48. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

50. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
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08 July 2005

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